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COUGHLAN, PETER D	

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2129	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/773,050	SALAM ET AL.	
	Examiner	Art Unit	
	Peter Coughlan	2129	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 February 2004* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/4/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. Claims 1-42 are pending in this application.

Specification Objections

2. The specification is rejected due to the following. Claim 3 uses the term "continuous-time". This could have a number of meanings including "real time" abilities but none are addressed or explained in the specification.

The specification is rejected due to the following. Claim 4 uses the term "interconnection structure" but no defined structure is stated.

The specification is rejected due to the following. Claim 5 uses the term "quadrant multiplier". The function or purpose of a 'quadrant multiplier' is not stated but the fact it exists is the only mention of it in the specification.

The specification is rejected due to the following. Claim 6 uses the term "transconductance". This purpose of function of a 'transconductance' is not clearly explained in the specification

Per the MPEP, section 608.01(l) the claim(s) is/are treated on its merits and a requirement made to amend the drawing and description to show the subject matter.

35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1-42 are rejected under 35 U.S.C. 101 for nonstatutory subject matter. The computer system must set forth a practical application of that § 101 judicial exception to produce a real-world result. Benson, 409 U.S. at 71-72, 175 USPQ at 676-77. The invention is ineligible because it has not been limited to a substantial practical application. A self programmable chip is a abstract idea and it does not have a practical application The result has to be a practical application. Please see the interim guidelines for examination of patent applications for patent subject matter eligibility published November 22, 2005 in the official gazette.

In determining whether the claim is for a "practical application," the focus is not on whether the steps taken to achieve a particular result are useful, tangible and concrete, but rather that the final result achieved by the claimed invention is "useful, tangible and concrete." If the claim is directed to a practical application of the § 101 judicial exception producing a result tied to the physical

world that does not preempt the judicial exception, then the claim meets the statutory requirement of 35 U.S.C. § 101.

The phrase 'synaptic cell with on-chip learning and synaptic weight storage integrated' has no real world practical application. There needs to be a real world function or purpose for the invention. If it to be used in health diagnostics, equipment failure tracking and prediction, or financial forecasting such results have not been claimed.

The invention must be for a practical application and either:

1) specify transforming (physical thing) or

2) have the FINAL RESULT (not the steps) achieve or produce a

useful (specific, substantial, AND credible),

concrete (substantially repeatable/ non-unpredictable), AND

tangible (real world/ non-abstract) result.

A claim that is so broad that it reads on both statutory and non-statutory subject matter, must be amended, and if the specification discloses a practical application but the claim is broader than the disclosure such that it does not require the practical application, then the claim must be amended.

Claims that detail a programmable chip or a programmable filter are not statutory.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4, 8-14, 17-19, 23, 25, 26, 28-34, 36, 38, 39, 41, 42 are rejected under 35 U.S.C. 102(e) (hereinafter referred to as **Winder**) being anticipated by Winder, U. S. Patent 6213958.

Claim 1

Winder anticipates a reconfigurable array processing network, providing (**Winder,** C12:14-22; 'Reconfigurable' of applicant is equivalent to 'self-learning' of Winder.): (a) a feed-forward neural network (**Winder,** C12:29-40); and (b) learning modules; and at least one control block providing digital memory (**Winder,** C5:2-41; 'Digital memory' of applicant is equivalent to 'ROM' of Winder.)and at least one control module supplying ordered signal routing functionality for said processing network. (**Winder,** C6:30-39; 'Routing functionality' of applicant is equivalent to 'bus' of Winder.)

Claim 2

Winder anticipates the chip has a mixed-mode design. (**Winder,** C5:20-41 and C7:26-35; 'Mixed mode" of applicant is equivalent to 'analog' and 'digital' of Winder.)

Claim 3

Winder anticipates the forward network (**Winder,** C12:29-40) and learning modules process in analog continuous-time mode (**Winder,** C7:26-35; 'Continuous-time' of applicant is illustrated by feedforward and analog-digital conversions of Winder.), while the parameters are stored on chip in digital form. (**Winder,** C5:2-41; 'Digital form' of applicant is equivalent to 'ROM' of Winder.)

Claim 4

Winder anticipates said processing network includes a first interconnection structure. (**Winder**, abstract; 'Interconnection structure' of applicant is equivalent to 'neural network' of Winder.)

Claim 8

Winder anticipates the plurality of control blocks includes a second interconnection structure. (**Winder,** C12:59-60; 'Second interconnection structure' of applicant is equivalent to 'classification' module of Winder.)

Claim 9

Winder anticipates the plurality of control blocks includes a plurality of D-Flip-flops operably coupled to said second interconnection structure. (**Winder,** C12:59-60; The classification module is connected to the neural network. The neural network holds weight values. The circuit that holds a single bit value is a d-flip-flop, thus d-flip-flop is connected to the second interconnection structure.)

Claim 10

Winder anticipates the plurality of control blocks includes a plurality of analog to digital converters operably coupled to said second interconnection structure. (**Winder,** C7:26-35)

Claim 11

Winder anticipates the plurality of control blocks includes a plurality of multiplying digital to analog converters operably coupled to said second interconnection structure. (**Winder,** C7:26-35)

Claim 12

Winder anticipates the plurality of control blocks includes a plurality of comparators operably coupled to said second interconnection structure and operable to perform parameter storage (**Winder,** C4:30-44; 'Parameter storage' of applicant is performed by 'memory' of Winder.) and analog to digital conversions. (**Winder,** C7:26-35)

Claim 13

Winder anticipates a communications medium operable to transmit input target data (**Winder,** C6:30-39; 'Communications medium' of applicant is equivalent to 'bus' of Winder.); learning hardware operable to compute synaptic weights based on the input target data (**Winder,** C8:11-24; 'Learning' of applicant occurs in 'learning mode' of Winder.); and a storage medium operable to store the computed weights (**Winder,** C5:2-41; 'Storage medium' of applicant is equivalent to 'ROM' of Winder.), wherein the synaptic cell is implemented in hardware on a single chip. (**Winder,** C5:20-41; 'Single chip' of applicant is equivalent to 'VLSI" of Winder.)

Claim 14

Winder anticipates said communications medium comprises an interconnect data bus. (**Winder,** C6:30-39; 'Interconnection data bus' of applicant is equivalent to 'bus' of Winder.)

Claim 17

Winder anticipates in communication with an analog to digital converter operable to convert the weights to digital form. (**Winder,** C7:26-35)

Claim 18

Winder anticipates said storage medium comprises a plurality of data flip-flops operable to store the computed weights in digital form. (**Winder,** C12:59-60;

The neural network holds weight values. The circuit that holds a single bit value is a d-flip-flop, and a series of 8 'd-flip-flops' is a byte which is 'digital form' of applicant.)

Claim 19

Winder anticipates a chip substrate providing a transmission medium (**Winder,** C6:30-39; 'Transmission medium' of applicant is equivalent to 'bus' of Winder.); a plurality of synaptic cells implemented on said chip substrate with on-chip learning and weight storage integrated therein (**Winder,** C8:11-24; 'Learning' of applicant occurs in 'learning mode' of Winder.); and at least one control cell implemented on said chip substrate and operable to route signals to and from said plurality of synaptic cells in an ordered fashion. (**Winder,** C6:30-39; 'Rout signals' of applicant is accomplished by 'bus' of Winder.)

Claim 23

Winder anticipates said synaptic cell comprises an analog to digital converter operable to convert the weights to digital form. (**Winder,** C7:26-35)

Claim 25

Winder anticipates said storage medium comprises a plurality of data flip-flops operable to store the computed weights in digital form. (**Winder,** C12:59-60; The neural network holds weight values. The circuit that holds a single bit value

is a d-flip-flop, and a series of 8 'd-flip-flops' is a byte which is 'digital form' of applicant.)

Claim 26

Winder anticipates said chip substrate comprises an interconnect having a data bus. (**Winder,** C6:30-39; 'Data bus' of applicant is equivalent to 'bus' of Winder.)

Claim 28

Winder anticipates activating a learning mode (**Winder,** C8:11-24; 'Learning' of applicant occurs in 'learning mode' of Winder.); activating a storage mode (**Winder,** C5:2-41; 'Storage mode' of applicant is illustrated by "RAM' and 'ROM' of Winder.); and activating a process mode. (**Winder,** abstract; 'Process mode' of applicant is equivalent to 'analyzing AE signals' of Winder.)

Claim 29

Winder anticipates activating a program mode. (**Winder,** abstract; 'Program mode' of applicant is equivalent to 'data acquisition performs sensitive and reliable clinical data acquisition, localization and classification' of Winder.)

Claim 30

Winder anticipates said activating a program mode comprises activating a program mode, wherein the chip accomplishes weight read out. (**Winder,**

abstract; By using a neural network, Winder uses weights that are part of the output.)

Claim 31

Winder anticipates said activating a program mode comprises activating a program mode, wherein the chip accomplishes weight read in. (**Winder,** C8:11-24; 'Weight read in' of applicant is equivalent to 'training mode' of Winder.)

Claim 32

Winder anticipates said activating a program mode comprises activating a program mode, wherein the chip accomplishes weight read in, wherein the weight read in signifies programming the weights for applications where the chip has already been trained. (**Winder,** abstract; 'Program mode' of applicant is equivalent to results of an output of a 'neural network' which uses trained weights of Winder.)

Claim 33

Winder anticipates activating a learning mode comprises activating a learning mode that is purely analog. (**Winder,** C12:29-58; 'Purely analog' of applicant is equivalent to 'AE (acoustic emission)' of Winder.)

Claim 34

Winder anticipates said activating a learning mode comprises activating a learning mode, wherein the chip activates a learning process based on inputs and desired output targets supplied by at least one of an application and a user. (**Winder,** C8:11-24; 'Inputs and desired output targets' of applicant is equivalent to 'classification in accordance with previously learned data' of Winder.)

Claim 36

Winder anticipates said activating a storage mode comprises activating a storage mode, wherein a user, once satisfied with performance of a chip network in the learning mode, saves computed weights in on-chip static digital memory. (**Winder,** C5:2-41; 'Static digital memory' of applicant is equivalent to 'ROM' of Winder.)

Claim 38

Winder anticipates activating a process mode comprises activating a process mode, wherein outputs are generated by a chip forward network. (**Winder,** C12:29-40; 'Chip forward network' of applicant is equivalent to 'feed-forward neural network' of Winder.)

Claim 39

Winder anticipates providing a chip substrate having a databus (**Winder,** C6:30-39; 'Databus' of applicant is equivalent to 'bus' of Winder.); operably attaching a plurality of synaptic cells to the chip substrate, wherein the synaptic

cells have on-chip learning and synaptic weight storage integrated therein (**Winder,** C8:11-24; 'Learning' of applicant occurs in 'learning mode' of Winder.); and operably attaching at least one control cell to the chip substrate, wherein the control cells are operable to route signals in an ordered fashion. (**Winder,** C6:30-39; 'Rout signals' of applicant is accomplished by 'bus' of Winder.)

Claim 41

Winder anticipates operably attaching an analog to digital converter to the chip substrate in the vicinity of the capacitor, wherein the analog to digital converter is operable to convert the synaptic weight to digital form (**Winder,** C7:26-35); and operably attaching at least one data flip-flop to the chip substrate in the vicinity of the analog to digital converter, wherein the data flip-flop is operable to store the synaptic weight in digital form. (**Winder,** C12:59-60; The neural network holds weight values. The circuit that holds a single bit value is a d-flip-flop, and a series of 8 'd-flip-flops' is a byte which is 'digital form' of applicant.)

Claim 42

Winder anticipates a chip substrate providing a transmission medium (**Winder,** C6:30-39; 'Transmission medium' of applicant is equivalent to 'bus' of Winder.); a programmable filter structure implemented on said chip substrate and operable to receive an input signal, filter the input signal according to predetermined weights, and output the filtered signal, said programmable filter

structure comprising: (a) an input operable to receive data comprising predetermined weights (**Winder,** C7:47-58; 'receive data' of applicant is equivalent to 'input data signals' of Winder.); (b) a storage medium operable to store the predetermined weights (**Winder,** C5:2-41; 'Storage medium' of applicant is equivalent to 'ROM' of Winder.); and (c) an output operable to communicate stored weights off chip. (**Winder,** C12:29-40; 'Output' of applicant is equivalent to 'output layer' of Winder.)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5, 6, 16, 22, 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Winder as set forth above, in view of Salam. (U. S. Patent 5689621, referred to as **Salam**)

Claim 5

Winder fails to particularly call for said processing network includes a plurality of 4-quadrant multipliers operably coupled to said first interconnection structure.

Salam teaches said processing network includes a plurality of 4-quadrant multipliers operably coupled to said first interconnection structure. (**Salam,** C6:37-49) It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify the teachings of Winder by dividing the chip into 4 major sub-function blocks as taught by Salam to have said processing network includes a plurality of 4-quadrant multipliers operably coupled to said first interconnection structure.

For the purpose of placing a major sub-function on a chip.

Claim 6

Winder fails to particularly call for said processing network includes a plurality of transconductance amplifiers operably coupled to said first interconnection structure.

Salam teaches said processing network includes a plurality of transconductance amplifiers operably coupled to said first interconnection structure. (**Salam,** C7:12-19) It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify the teachings of Winder by dividing the chip into 4 major sub-function blocks as taught by Salam to have said processing network includes a plurality of transconductance amplifiers operably coupled to said first interconnection structure.

For the purpose of placing a second major sub-function on a chip.

Claim 16

Winder fails to particularly call a plurality of one-dimension multipliers.

Salam teaches a plurality of one-dimension multipliers. (**Salam,** C5:33-46) It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify the teachings of Winder by employing multipliers for the neural network to function as taught by Salam to have a plurality of one-dimension multipliers.

For the purpose of fulfilling the multiplication needs for the functioning of a neural network.

Claim 22

Winder fails to particularly call for said learning hardware comprises a plurality of one-dimension multipliers.

Salam teaches said learning hardware comprises a plurality of one-dimension multipliers. (**Salam,** C5:33-46) It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify the teachings of Winder by employing multipliers for the neural network to function as taught by Salam to have said learning hardware comprises a plurality of one-dimension multipliers.

For the purpose of fulfilling the multiplication needs for the functioning of a neural network.

Claim 35

Winder fails to particularly call for said activating a storage mode comprises activating a storage mode that is analog-digital.

Salam teaches said activating a storage mode comprises activating a storage mode that is analog-digital. (**Salam,** abstract; 'Storage mode that is analog-digital' of applicant is illustrated by the performance of the 'weight updating circuit' of Salam.) It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify the teachings of Winder by using storage or memory for holding values as taught by Salam to have said activating a storage mode comprises activating a storage mode that is analog-digital.

For the purpose of holding weight values, incoming data values, or product values for the neural network.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7, 15, 20, 21, 24, 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Winder as set forth above, in view of Thaler. (U. S. Patent 6014653, referred to as **Thaler**)

Claim 7

Winder fails to particularly call for said processing network includes a plurality of active load resistances operably coupled to said first interconnection structure.

Thaler teaches said processing network includes a plurality of active load resistances operably coupled to said first interconnection structure. (**Thaler,** C8:16-30; 'Plurality of active load resistances' of applicant is equivalent to 'resistors' of Thaler.) It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify the teachings of Winder by using load resistances as taught by Thaler to have said processing network includes a plurality of active load resistances operably coupled to said first interconnection structure.

For the purpose of using hardware where there exists no mathematical model.

Claim 15

Winder fails to particularly call for said learning hardware comprises a capacitor.

Thaler teaches said learning hardware comprises a capacitor. (**Thaler;** C8:16-30) It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify the teachings of Winder by using a capacitor's output as input for another device as taught by Thaler to have said learning hardware comprises a capacitor.

For the purpose of obtaining another established device for a neural network

Claim 20

Winder fails to particularly call for at least one synaptic cell of said plurality of synaptic cells comprises learning hardware operable to compute weights based on input target data.

Thaler teaches at least one synaptic cell of said plurality of synaptic cells comprises learning hardware operable to compute weights based on input target data. (**Thaler,** C4:9-25; 'Compute weights' of applicant is equivalent to 'adjust the weights' of Thaler.) It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify the teachings of Winder by generating the value of weights as taught by Thaler to have at least one synaptic cell of said plurality of synaptic cells comprises learning hardware operable to compute weights based on input target data.

For the purpose of the neural network being able to train itself

Claim 21

Winder fails to particularly call for said learning hardware comprises a capacitor.

Thaler teaches said learning hardware comprises a capacitor. (**Thaler;** C8:16-30) It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify the teachings of Winder by having a capacitor as part of the neural network as taught by Thaler to have said learning hardware comprises a capacitor.

For the purpose of holding a charge that can be used in further operations of the neural network.

Claim 24

Winder fails to particularly call for at least one synaptic cell of said plurality of synaptic cells comprises a storage medium operable to store computed weights.

Thaler teaches at least one synaptic cell of said plurality of synaptic cells comprises a storage medium operable to store computed weights.(**Thaler,** C7:23-41; Thaler states that there exists weights, therefore they must be stored in a given medium to exist. 'Synaptic cells' of applicant is equivalent to 'neurons' of Thaler.) It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify the teachings of Winder by using memory to contain the weights for the neural network as taught by Thaler to have at least one synaptic cell of said plurality of synaptic cells comprises a storage medium operable to store computed weights.

For the purpose of the neural network to use the weights at a given time so that the neural network does not have to retrained ever time.

Claim 37

Winder fails to particularly call for said activating a storage mode comprises automatically activating a storage mode after passage of a predetermined amount of time since activation of the learning mode.

Thaler teaches said activating a storage mode comprises automatically activating a storage mode after passage of a predetermined amount of time since activation of the learning mode. (**Thaler,** C19:12-30; 'Passage of a predetermined amount of time' of applicant is equivalent to 'predetermined level' of Thaler.) It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify the teachings of Winder by using time as a parameter for activation of the learning mode as taught by Thaler to have said activating a storage mode comprises automatically activating a storage mode after passage of a predetermined amount of time since activation of the learning mode.

For the purpose of avoiding wasting time by not converging to a given point within a given segment of time.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Winder as set forth above, in view of Greenberger. (U. S. Patent 6675187, referred to as **Greenberger**)

Claim 27

Winder fails to particularly call for plurality of synaptic cells and a plurality of said control cells is organized into an array structure comprising identical cells of 17 X16 synaptic cells augmented by a column of control cells, the chip further comprising decoders and de-multiplexers operable to provide chip level programming of synaptic weights for multiple blocks in parallel, said decoders and demultiplexers used for both row and column selections.

Greenberger teaches plurality of synaptic cells and a plurality of said control cells is organized into an array structure comprising identical cells of 17.times.16 synaptic cells augmented by a column of control cells (**Greenberger,** C21 through C31; Greenberger illustrates a 17 X 16 array.), the chip further

comprising decoders and de-multiplexers operable to provide chip level programming of synaptic weights for multiple blocks in parallel, said decoders and demultiplexers used for both row and column selections. (**Greenberger,** C11:11-18; 'Demultiplexers' of applicant is equivalent to 'multiplexers' of Greenberger.) It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify the teachings of Winder by using multiplexers for encoding and decoding as taught by Greenberger to have plurality of synaptic cells and a plurality of said control cells is organized into an array structure comprising identical cells of 17 X 16 synaptic cells augmented by a column of control cells, the chip further comprising decoders and de-multiplexers operable to provide chip level programming of synaptic weights for multiple blocks in parallel, said decoders and demultiplexers used for both row and column selections.

For the purpose of being able to change the programming width and depth of a neural network by the use of the multiplexers.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary

skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over Winder as set forth above, in view of Thaler and further in view of Salam. (U. S. Patent 6014653, referred to as **Thaler;** U. S. Patent 5689621, referred to as **Salam**)

Claim 40

Winder fails to particularly call for operably attaching a capacitor to the chip substrate; and operably attaching a plurality of one-dimension multipliers to the chip substrate in the vicinity of the capacitor; and interconnecting the capacitor and the one dimensional multipliers in a configuration causing the plurality of the one-dimension multipliers to scale an input target signal, while the capacitor allows a voltage of the input target signal to cause a synaptic weight to settle over time.

Thaler teaches operably attaching a capacitor to the chip substrate. (**Thaler;** C8:16-30) It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify the teachings of Winder by making the capacitor as part of the chip as taught by Thaler by attaching a capacitor to the chip substrate.

For the purpose of the capacitor to be part of a chip so that it's output can be another components input.

Salam teaches operably attaching a plurality of one-dimension multipliers to the chip substrate in the vicinity of the capacitor (**Salam,** C5:33-46); and interconnecting the capacitor and the one dimensional multipliers in a configuration causing the plurality of the one-dimension multipliers to scale an input target signal, while the capacitor allows a voltage of the input target signal to cause a synaptic weight to settle over time. (Using the capacitor to hold a charge that can be used as input to a multiplier is common in the art.) It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify the teachings of Winder by using two hardware devices that are used by one another, keeping them in a close vicinity of one another as taught by Salam by attaching a plurality of one-dimension multipliers to the chip substrate in the vicinity of the capacitor; and interconnecting the capacitor and the one dimensional multipliers in a configuration causing the plurality of the one-dimension multipliers to scale an input target signal, while the capacitor allows a voltage of the input target signal to cause a synaptic weight to settle over time.

For the purpose of keeping both devices on the same chip they have to within a 'vicinity' of one another.

Conclusion

5. The prior art of record and not relied upon is considered pertinent to the applicant's disclosure.

-U. S. Patent 6691073: Erten

-U. S. Patent 6735482: Erten

-U. S. Patent 6768515: Erten

-U. S. Patent Publication 20030006809: Enriquez

-U. S. Patent Publication 20020072769: Silvian

-U. S. Patent Publication 20020032570: Kub

-U. S. Patent 6207936: de Waard

-U. S. Patent 6092017: Ishida

-U. S. Patent 6084981: Horiba

-U. S. Patent 6216663: Kato

-U. S. Patent 5321342: Kruse

-U. S. Patent 5303329: Mead

-U. S. Patent 4293920: Merola

6. Claims 1-42 are rejected.

Correspondence Information

7. Any inquiry concerning this information or related to the subject disclosure should be directed to the Examiner Peter Coughlan, whose telephone number is (571) 272-5990. The Examiner can be reached on Monday through Friday from 7:15 a.m. to 3:45 p.m.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor David Vincent can be reached at (571) 272-3687. Any response to this office action should be mailed to:

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Peter Coughlan

8/14/2006